B.SC. 5 SEM PHYSICS 2025-26

SKELETON PRACTICAL PAPER

QUESTION

i) Diagram

ii) Apparatus

iii) Theory

iv) Observation

v) Observation table

vi) Calculation

vii) Result

viii) Precautions

CHOOSE ANY 1 QUESTION IN PER STUDENT

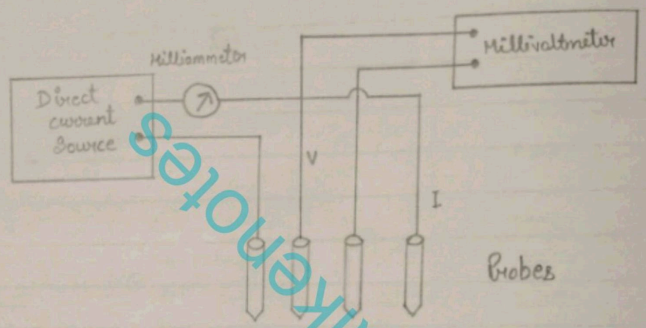
1 Study the characteristics of a given transistor (PNP/NPN) in common emitter, common base, and common collector configurations.

2 Study the characteristics of a junction diode and a Zener diode

3 Study the characteristics of a field effect transistor (FET) and design an amplifier withfinite gain

4 Study OR, AND, and NOT logic gates using discrete components and compare them with TTL integrated circuits (ICs)

5 Study the temperature dependence of resistance in a semiconductor using the four-probe method.



Circuit used for Resistivity measurements

Date

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Object – Study of temperature dependence of resistance of a semiconductor using four probe method.

Apparatus – Probes arrangement, sample, oven, thermometer four probe setup, constant current generation.

Theory and formula –

Four sharp probes are placed on a flat surface of the material to be measured current is passed through the two outer electrodes and the floating potential is measured across the inner pair.

four probes are spaced S_1, S_2 and S_3 apart current I is passed through the outer probes 1 and 4 and the floating potential V is measured across the inner pair of probes (2 and 3).

When the points spacing equal

$$S_1 = S_2 = S_3 = S_4$$

We get resistivity (ρ_0)

$$\rho_0 = \frac{V}{I} \times 2\pi S$$

Here, v = floating potential difference between inner probe in V

I = Current through the outer pair of probes in the width of slice is ω

S = Spacing between the probes in meters

Resistivity –

$$\rho = \frac{\rho_0}{G_7(\omega/s)}$$

Wonder

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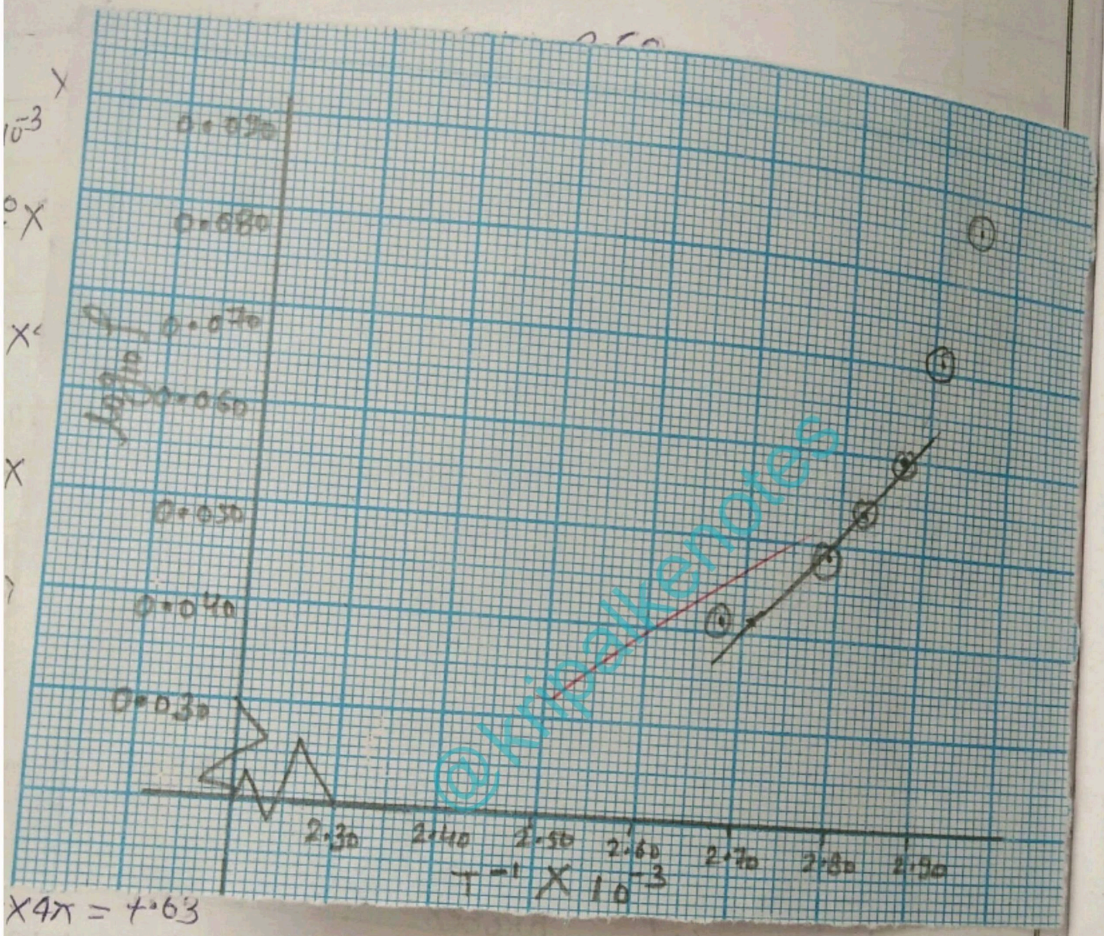
$\times 2\pi S$



$\times 4\pi = 7.63$

$= \left[\omega/s = \frac{0.5}{2} = 0.25\right]$

$G_7(\omega/s) = 6.93$

$\rho_7 = \frac{7.62}{6.93} = 1.10$

Expt.

S.No.
1.
2.
3.
4.
5.
6.
7.
8.
1.
2.

Calculation —

$$f_0 = \frac{V}{I} \times 2\pi S$$

$$f_0 = \frac{1.76}{2.6 \times 10^{-3}} \times 2\pi \times 2 \times 10^{-3} = \frac{1.76 \times 4\pi}{2.6} = 8.50$$

$$f_0 = \frac{1.70}{2.6} \times 4\pi = 8.21$$

$$f_0 = \frac{1.66}{2.6} \times 4\pi = 8.01$$

$$f_0 = \frac{1.63}{2.6} \times 4\pi = 7.87$$

$$f_0 = \frac{1.61}{2.6} \times 4\pi = 7.77$$

$$f_0 = \frac{1.60}{2.6} \times 4\pi = 7.72$$

$$f_0 = \frac{1.59}{2.6} \times 4\pi = 7.68$$

$$f_0 = \frac{1.58}{2.6} \times 4\pi = 7.63$$

$$f = \frac{f_0}{G_7(\omega/S)} = \left[\omega/3 = \frac{0.5}{2} = 0.25\right]$$

$$G_7(\omega/S) = 6.93$$

$$f_1 = \frac{8.50}{6.93} = 1.22$$

$$f_2 = \frac{8.21}{6.93} = 1.18$$

$$f_3 = \frac{8.01}{6.93} = 1.15$$

$$f_4 = \frac{7.87}{6.93} = 1.13$$

$$f_5 = \frac{7.77}{6.93} = 1.12$$

$$f_6 = \frac{7.72}{6.93} = 1.11$$

$$f_7 = \frac{7.68}{6.93} = 1.10$$

$$f_8 = \frac{7.63}{6.93} = 1.10$$

Date

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Observation –

Distance between probes $s = 2mm = 2 \times 10^{-3} m$.

Thickness of the crystal $w = 0.5mm = 5 \times 10^{-4} m$.

Observation table –

S.No.	Temperature(°C)	Volts(V)	Temp.(K)	ρ (Ω/cm)	$T^{-1} \times 10^{-3}$	$\log_{10} \rho$
1.	65	1.762	338	1.22	2.95	0.086
2.	70	1.704	343	1.18	2.91	0.071
3.	75	1.664	348	1.15	2.87	0.060
4.	80	1.638	353	1.13	2.83	0.053
5.	85	1.616	358	1.12	2.79	0.049
6.	90	1.601	363	1.11	2.75	0.045
7.	95	1.596	368	1.10	2.71	0.041
8.	100	1.584	373	1.10	2.68	0.041

Result –

We obtain the graph for this.

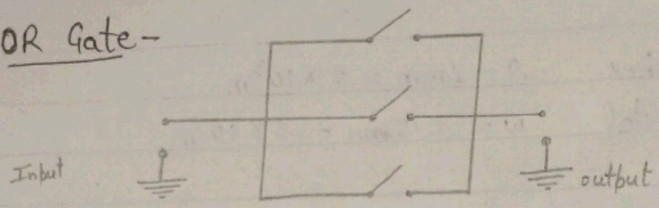
Precaution –

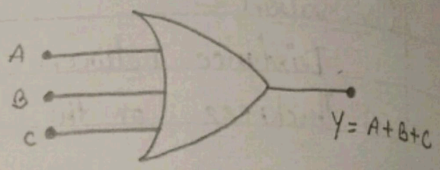
1. Wires should be tightly connected
2. Current should be constant.
3. Carefully notedown thermometer reading.

Namita Khatri
31-05-21

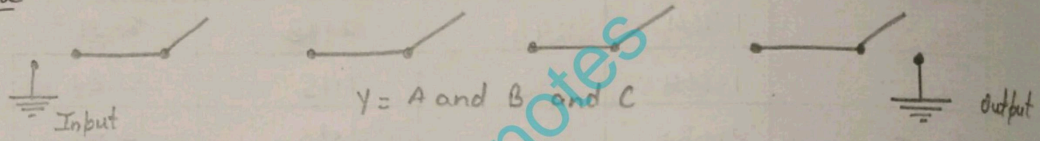
Teacher's Signature : .....

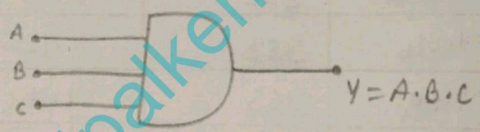
OR Gate -



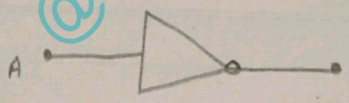


AND Gate -

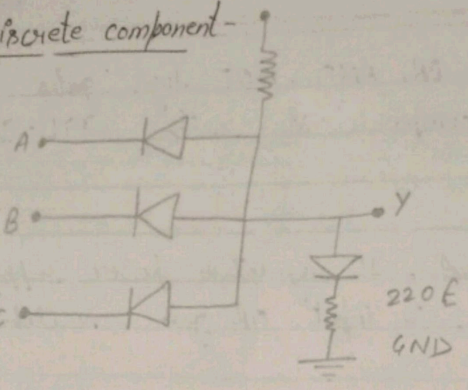




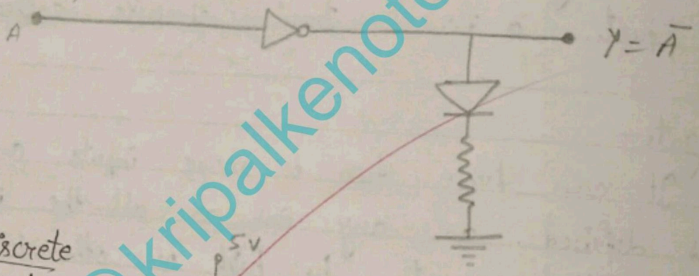
NOT Gate -



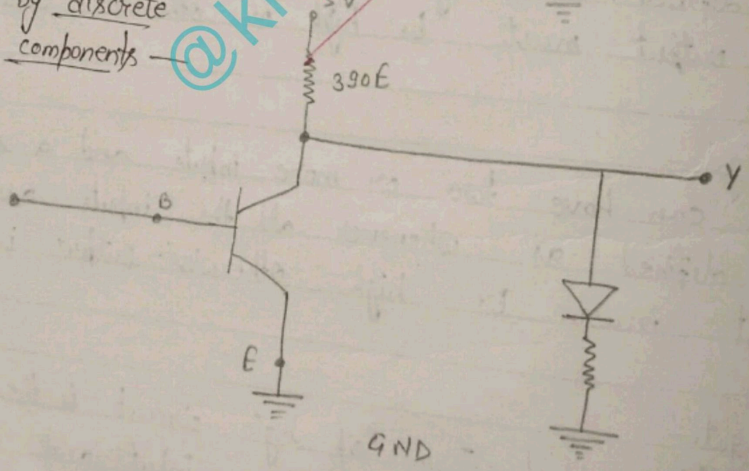
AND - Gate discrete component -



NOT - Gate by TTL (ICs) —



NOT - Gate by discrete components —



Date

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Expt. No. 2

Object - To study OR, AND, NOT logic gates using discrete compound and compare it with TTL - ICs.

Apparatus -

5V at 100mA, IC regulated power supply, NOT gate, 3 input AND gate, 3 input OR gate, switch, LED patch corale.

Theary -

All digital equipments, simple or complex is constituted from just a few basic circuits called logic elements.

OR gate -

It can have two or more inputs and a single output. It is defined as any one or all the inputs are high then output must be high or otherwise low.

AND gate -

It can have two or more inputs and a single output. It is defined as whenever all the inputs are high, then output must be high otherwise output is low.

NOT gate -

The simplest form of logic circuit is the inverter or NOT gate. It can have one input and one output terminal.

Wonder

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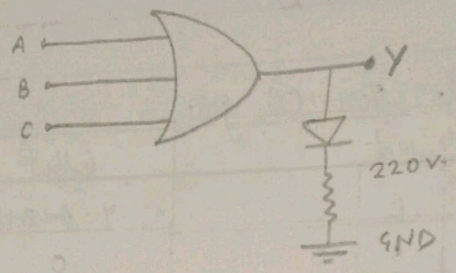
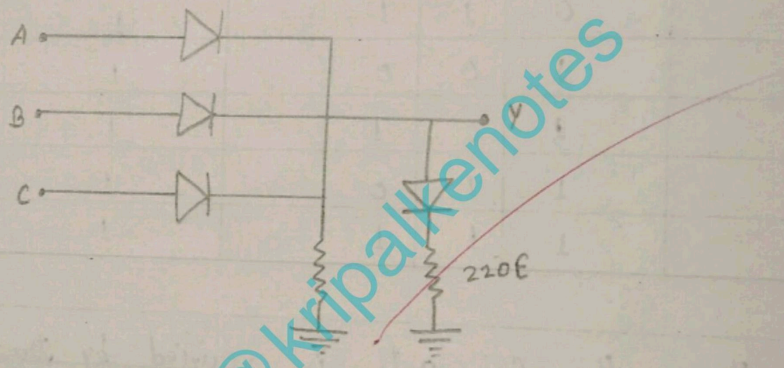
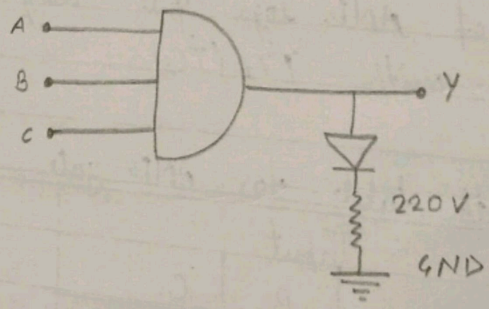
OR gate by TTL (ICs) –



OR-gate by discrete component –



AND gate by TTL (ICs) –



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Expt. No.

Object-1. Study of OR logic gate using discrete components and comparison with TTL (ICs)

Observation- Truth table for OR gate

S.No.	Input			Output
	A	B	C	Y = A+B+C
1.	0	0	0	0
2.	0	0	1	1
3.	0	1	0	1
4.	0	1	1	1
5.	1	0	0	1
6.	1	0	1	1
7.	1	1	0	1
8.	1	1	1	1

Result - Hence the OR gate is verified by truth table.

Object-2. Study of AND logic gate using discrete components in comparison with TTL (ICs)

Observation- Truth table for AND gate

S.No.	Input			Output
	A	B	C	Y = A·B·C
1.	0	0	0	0
2.	0	0	1	0
3.	0	1	0	0
4.	0	1	1	0
5.	1	0	0	0

Wonder

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Date

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Expt. No.

6.	1	0	1	0
7.	1	1	0	0
8.	1	1	1	1

Result- The AND logic gate is verified by truth table

Object 3. Study of NOT logic gate using discrete components in comparison with TTL (ICs)

Observation- Truth table for NOT gate

S.No.	Input	Output
	A	$Y = \bar{A}$
1.	0	1
2.	1	0

Result - The NOT logic gate is verified by truth table.

Precautions-

1. Connect the wires properly.
2. Power supply should not exceed 5V.

31-03-21

Wonder

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Object - To study and plot the forward and reverse bias (Breakdown) Characteristic zener diode.

Apparatus required —

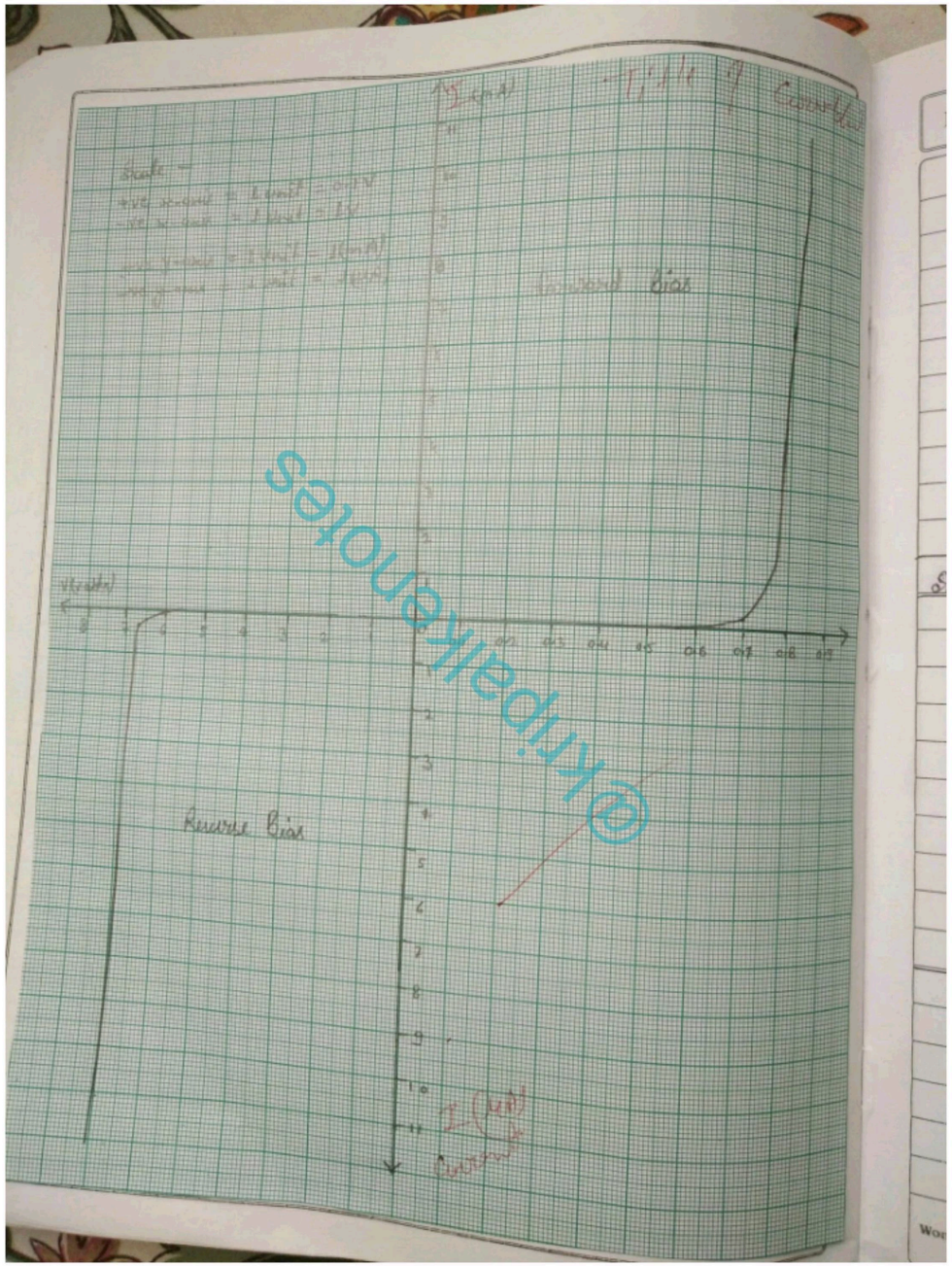
Junction and zener diode, a low current, low voltage, d.c. source, battery eliminator of 0.15 volt, a miliammeter and a micro-ammeter of suitable ranges rheostat, Patch chords. etc.

Theory —

Zener diode is a silicon diode that the manufacturer has optimised for operation in the breakdown region. It is the backbone of voltage regulation circuit that holds the load voltage almost constant despite large change in line voltage and load resistance.

In principle, if certain portion of I-V characteristic of any circuit element is such that inspite of change in voltage, current remains constant or inspite of change in current, voltage remains same i.e. the dynamic resistance becomes almost zero or infinity then such circuit elements can be used as voltage or current regulating circuit elements.

Since I-V characteristics of a zener diode in the breakdown region and output characteristics of common base transistor are of this nature, hence these can be used for regulation. Here we have described and study of zener diode I-V characteristics.



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for reverse biased characteristics of zenerdiode, almost no current flows through the diode till the zener voltage of the diode is reached at which there is a sudden increase in the current with the increase in applied voltage. The voltage across the diode remains constant at its zener voltage.

Observation Table —

1. for forward bias characteristics.

S.No.	V (volts) at 2V	I (current) at 20 mA
1.	0.1	0
2.	0.2	0
3.	0.3	0
4.	0.4	0
5.	0.5	0
6.	0.6	0
7.	0.7	0.2
8.	0.8	6.30
9.	0.83	16.00
10.	0.85	18.65

2. for Reverse bias characteristics —

Wonder

Teacher's Signature : _____

Date

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S.No	V (voltage) at 20V.	I (current) at 20 mA
1	1	0
2	2	0
3	3	0
4	4	0
5	5	0
6	6	0
7	6.50	0.01
8	6.65	0.03
9	7	15.36

Result – The forward and reverse bias breakdown characteristics of a zener diode as shown in graph.

Precautions of sources of error –

(i) Meters of proper range and least count should be used to measure forward and reverse currents.

(ii) The reverse voltage should not be increased beyond a certain limit otherwise current will suddenly increase and junction would be damaged permanently.

Navin Kakkar
02-09-2024

Wonder

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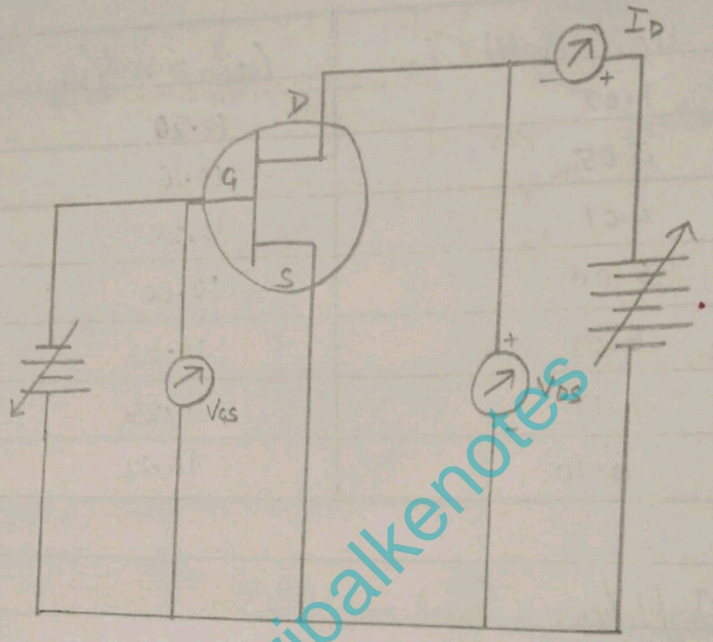

FET characteristics

V_{GS} = Gate source voltage

I_D = Drain current

V_{DS} = Drain source voltage

G = Gate

D = Drain

S = Source

Date

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Object - Study of field effect transistor characteristics.

Apparatus required - FET, voltmeter, ammeter, D.C power supply, connecting wires.

Theory and formula -

FET has high input impedance and field effect transister to control the current by application of an electric field across the conducting region since it is called unipolar device.

FET is semiconductor device which has 3 terminal gate (G), source (S) and drain (D).

FET consists of small bar of n- semiconductor and has (-ve) terminal of source and the terminal drain is a heavily doped gate electrode G of P material from junction on each side of bar- region between the junction is called channel.

The electrons flow from source to drain through a channel between the depletion layer hence in such a device the current increase up to a certain limit to the pinch off voltage.

$$\text{Drain Resistance } R_{ds} = \left|\frac{\Delta V_{ds}}{\Delta I_{ds}}\right|_{V_{GS} = \text{constant}}$$

$$\text{Transconductance for } g_m = \left|\frac{\Delta I_{DS}}{\Delta V_{GS}}\right|_{V_{DS} = \text{constant}}$$

Wonder

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Calculation –

1.) Drain resistance (r_{DS}) –

$$r_{DS} = \left(\frac{\Delta V_{DS}}{\Delta I_{DS}}\right)_{V_{GS}} = \text{Constant}$$

$$r_{DS} = \frac{1}{1.5} \times 10^3 = 0.66 \times 10^3 \Omega$$

2.) Trans conductance (g_m) –

$$g_m = \left(\frac{\Delta I_{DS}}{\Delta V_{GS}}\right)_{V_{DS}} = \text{Constant}$$

$$g_m = \frac{1.5}{0.2} \times 10^{-3} = 7.5 \times 10^{-3} \Omega$$

3.) Amplification factor (μ) –

$$\mu = r_{DS} \times g_m$$

$$= 0.66 \times 10^3 \times 7.5 \times 10^{-3} = 4.05$$

$$\mu = \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right)_{I_{DS}} = \text{Constant}$$

$$\mu = \frac{6}{0.2} = 30$$

Date

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The three terminal of FET are -

1. Source
2. Gate
3. Drain

Observation Table -

Table for I_D V/s V_{DS} for different fixed value of V_{GS}.

S.No.	V_{DS} (V)	Drain current I_D (in mA)						
		V_{GS} = 0V	V_{GS} = -0.5V	V_{GS} = -1V	-1.5V	-2V	-2.5V	-3V
1.	0	0	0.0	0	0	0	0	0
2.	0.5	2.24	1.74	1.49	0.94	0.47	0.05	0.01
3.	1.0	4.01	3.08	2.30	1.43	0.62	0.06	0
4.	1.5	5.30	4.00	2.83	1.64	0.66	0.07	0
5.	2.0	6.13	4.55	3.07	1.73	0.68	0.07	0
6.	2.5	6.60	4.82	3.18	1.77	0.70	0.07	0

Note - Do not increase V_{DS} beyond 7 volts

Object 2.

Drain current V/s gate bias characteristics.

S.No.	V_{GS} (V)	I_D (in mA)						
		V_{DS} = 18V	16V	12V	8V	4V	2V	1V
1.	0.0	6.25	6.40	6.53	6.60	6.86	5.96	4.05
2.	0.5	4.59	4.60	4.55	4.80	4.82	4.38	3.22
3.	1.0	3.17	3.13	3.15	3.30	3.20	3.00	2.39
4.	1.5	1.83	1.81	1.89	1.87	1.85	1.71	1.50
5.	2.0	0.76	0.78	0.60	0.70	0.74	0.68	0.62
	2.5	0.10	0.11	0.07	0.09	0.09	0.09	0.6

Wonder

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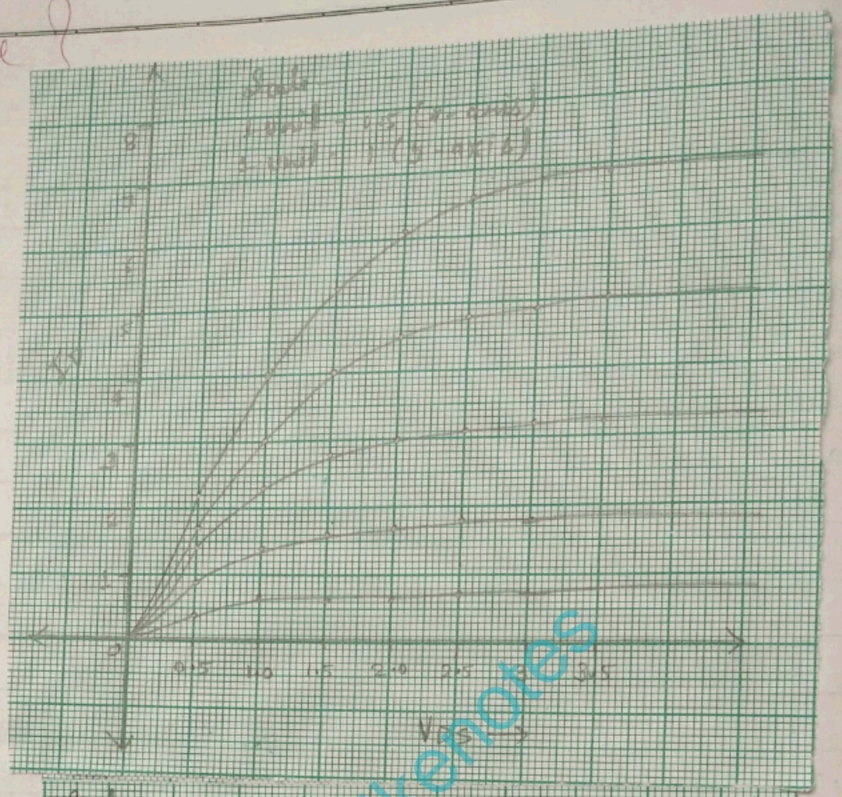
Title ?



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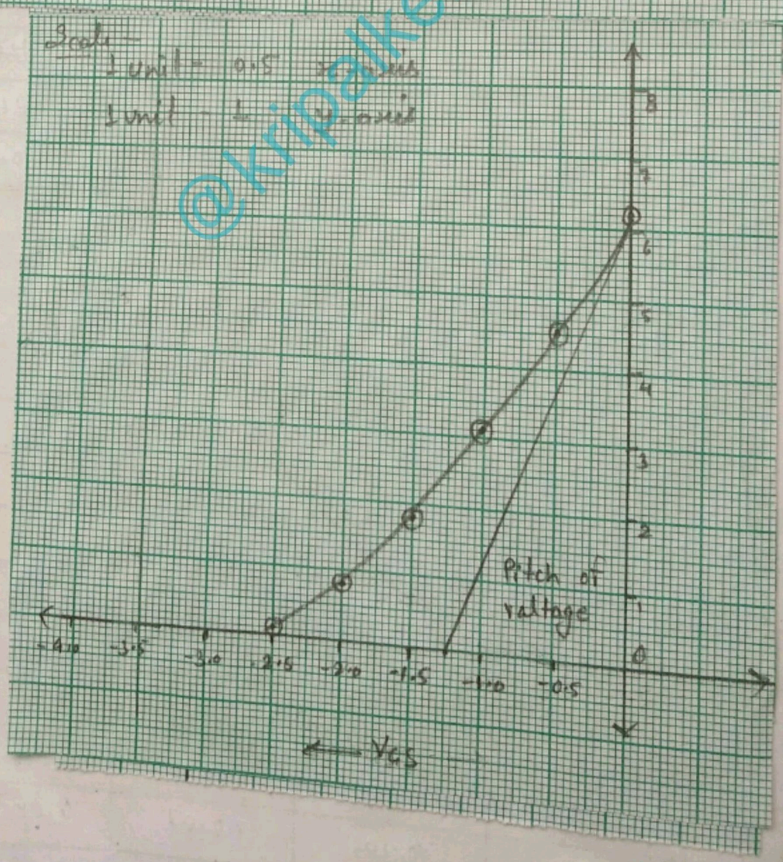

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Result -

The drain resistance $V_{DS} = 0.66 \times 10^3 \Omega$

Trans conductance $g_m = 7.5 \times 10^{-3} \Omega$

Amplification factor $\mu = 30$

Pitch of voltage = -1.25

Precautions -

1. Readings should be taken properly.
2. Wires should be connected carefully.

Verified
02-04-2024

Characteristic of PNP Tranistor in CB configuration

Object: To study the characteristic of PNP transistor in common base configuration.

Apparatus used: Transistor, variable DC source of range 0-3 volt and 0-15volts, voltmeter of range 0-3 and 0-15volt, mili-ammeter, wires/leads.

Theory: Transistor is an electronic component which is used in place of triode valve. It has application in amplification of signals, design of oscillators etc. It has three terminals which are termed as emitter, base and collector. It can be connected in circuit in three modes.

(1) Common base configuration

(2) Common emitter configuration and

(3) Common collector configuration.

According to two port analysis in terms of hybrid parameters, the input voltage (V_{EB}) and output current (I_C) are function of input current (I_E) and output voltage (V_{CB}) . i.e.

$$\left.\begin{aligned} V_{EB} &= h_{ib}\, I_E + h_{rb}\, V_{CB} \\ I_C &= h_{fb}\, I_E + h_{ob}\, V_{CB} \end{aligned}\right\} \qquad (1)$$

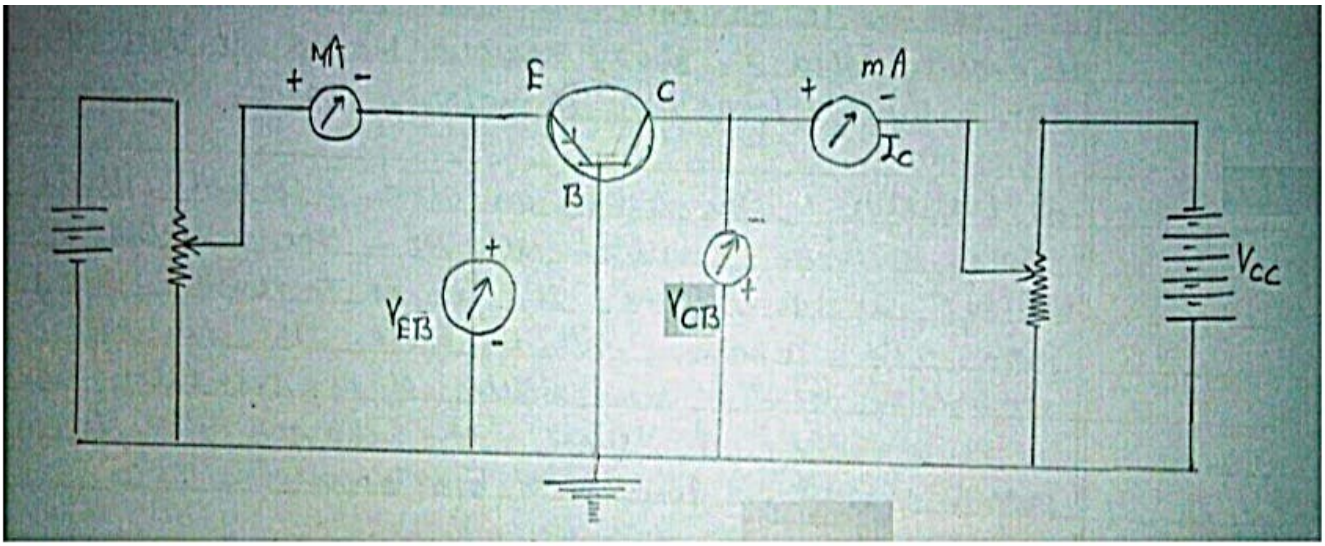
According to equation (1), there are four characteristic curves of transistor in common base configuration which are defined as follows.

(1) Input characteristic: The variation of input current (I_E) with input voltage (V_{EB}) at constant output voltage (V_{CB}) provides the input characteristics. Input resistance can be obtained by this characteristic curve.

(2) Output characteristic: The variation of output current (I_C) with output voltage (V_{CB}) at constant input current (I_E) provides the output characteristics. Output admittance and output resistance can be determined with help of this characteristic curve.

(3) Forward current transfer characteristic: The variation of output current (I_C) with input current (I_E) at constant output voltage (V_{CB}) provides the forward current transfer characteristics. The slop of curve gives the DC current gain in CB configuration.

(4) Reverse voltage transfer characteristic: The variation of input voltage (V_{EB}) with output voltage (V_{CB}) at constant input current (I_E) provides the reverse voltage transfer characteristics.



Observation:

A. Table for input characteristic

1. Least count of voltmeter= 0.02 V
2. Least count of ammeter= 1 mA

Sr. No.	V_{CB}=0volt		V_{CB}=8volt	
	V_{EB} (Volt)	I_E (mA)	V_{EB} (Volt)	I_E (mA)
1.	*0*	*0*	*0*	*0*
2.	*0.6*	*0*	*0.6*	*1*
3.	*0.62*	*1*	*0.62*	*2*
4.	*0.64*	*2*	*0.64*	*3*
5.	*0.66*	*4*	*0.66*	*5*
6.	*0.68*	*6*	*0.68*	*8*
7.	*0.7*	*9*	*0.7*	*10*
8.	*0.72*	*11*	*0.72*	*13*
9.	*0.74*	*14*	*0.74*	*16*
10.	*0.76*	*17*	*0.76*	*19*
11	*0.78*	*20*	*0.78*	*23*
12.	*0.8*	*23*	*0.8*	*26*
13.	*0.82*	*26*	*0.82*	*30*
14.	*0.84*	*29*	*0.84*	*33*
15.	*0.86*	*33*	*0.86*	*38*
16.	*0.88*	*37*	*0.88*	*42*
17.	*0.9*	*40*	*0.9*	*46*
18.	*0.92*	*43*	*0.92*	*49*

B. Table for Output characteristic

1. Least count of voltmeter= 0.2 V
2. Least count of ammeter= 1 mA

Sr. No.	V_{CB} *(volts)*	I_C (mA)			
		I_E=2 mA	I_E=4 mA	I_E=6 mA	I_E=8 mA
1.	0	1.8	3.8	5.8	7.8
2.	1	2.0	4.0	6.0	8.0
3.	2	2.0	4.0	6.0	8.0
4.	3	2.0	4.0	6.0	8.0
5.	4	2.0	4.0	6.0	8.0
6.	5	2.0	4.0	6.0	8.0
7.	6	2.0	4.0	6.0	8.0
8.	7	2.0	4.0	6.0	8.0
9.	8	2.0	4.0	6.0	8.0
10.	9	2.0	4.0	6.0	8.0

C. Table for forward current transfer characteristic

V_{CB}=2 volts =constant

Sr. No.	I_E *(mA)*	I_C *(mA)*
1.	0	0
2.	5	5
3.	10	10
4.	15	15
5.	20	19
6.	25	24
7.	30	29
8.	35	33
9.	40	38

***Result:* The following results can be written on the basis of characteristic curve.**

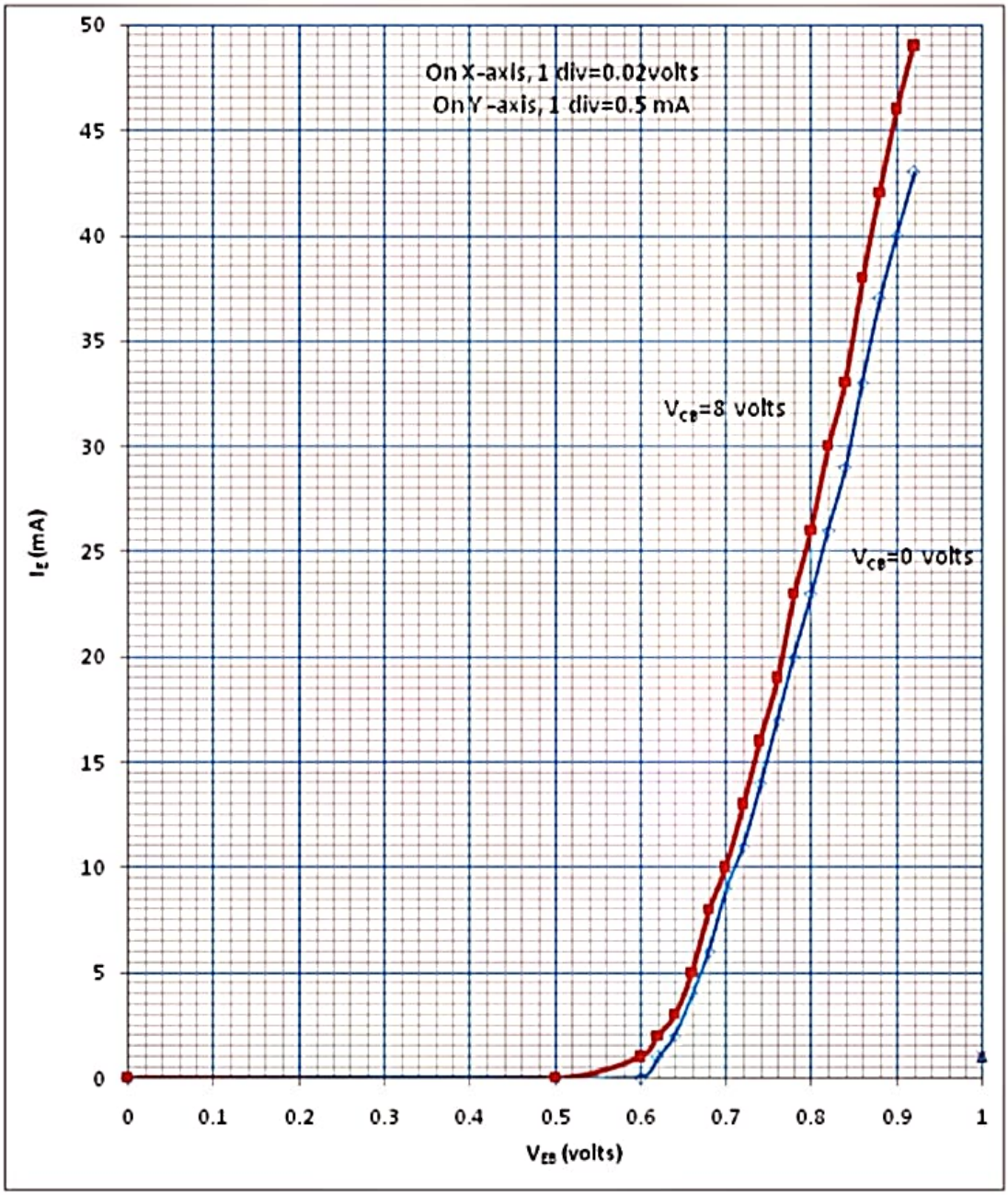
(A) Input characteristic curve shows that emitter current I_E increases rapidly with small increases in input voltage V_{EB} after knee voltage at constant output voltage. As output voltage V_{CB} made more negative, I_E rises more rapidly.

(B) Output characteristic curve shows that the output current I_C is approximately independent of output voltage V_{CB} at constant input current I_E . Even at zero output voltage, there is finite value of output current.

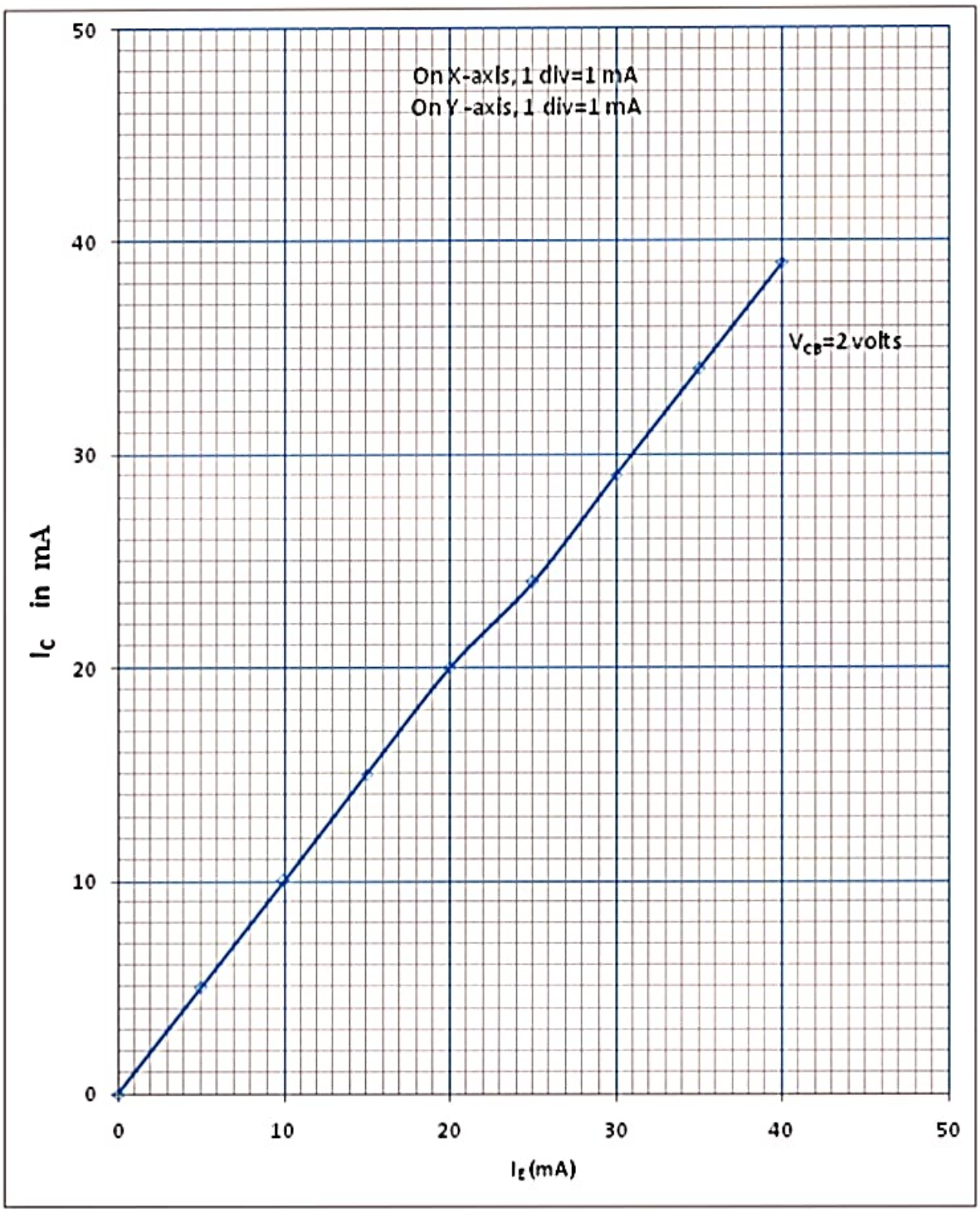
(C) The forward current transfer characteristic curve indicates that output current I_C is linearly related with input current I_E. But the value of I_C can not be greater than the I_E hence current gain will be less than 1.

Precautions:

1. The connection should be tight otherwise fluctuation in voltage and current will happen.
2. At the turning point of curve, more reading should be taken.
3. For the accuracy, current should be taken both in mA and μA..
4. The reading should be in multiple of least count.



Input characteristic Curve



Current Transfer characteristic Curve