Sec. B: Choose any 4 questions, choosing 1 question from each unit. Each question carries a mark weight of 15.

1 (A) State and establish the maximum power dissipation theorem. Obtain the proof for maximum power and find the maximum efficiency of such a circuit. 1 (B) State Norton's theory for circuit analysis and prove it.

2 (A) State and prove the reciprocity theorem. What is the internal impedance?

2 (B) Determine the DC voltage applied to any A junction when Js = 30 microA/cm2 and J = 2 A/cm2 are the normal values of the signals.

3 (A) Describe the input and output characteristics for a PNP transistor. Describe the experimental method for these characteristics. In a PNP transistor, define input, output, conducting base, current ratio, input impedance, and reverse voltage ratio for this circuit configuration. (RU
3 (B) For a transistor, the reverse saturation current is 0.15 mu A in the common base configuration and 20 mu A in the common emitter configuration. If the base current (I_B) is 10 mA, find the current gain \alpha and \beta.

4 (A) What do you understand by operating point Q and its stability? Define various stability coefficients. What do you understand by

thermal breakdown? How is an amplifier circuit protected from thermal breakdown? 4 (B) If the current gain of a transistor in the CB configuration is 0.98, find the current gain in the CE configuration and the CC configuration.

(A) How is an OP AMP used as an adder and a subtractor? Explain with a circuit diagram. 5 (B) The CMRR of a differential amplifier is 55 decibels. If its differential mode gain is 1200, calculate the common mode gain.

6 (A) Prove that negative gradation voltage increases the input impedance and decreases the output impedance of the feed-in amplifier. 6 (B) Find the value of gain. Also calculate the input impedance of the amplifier. The input and feed-in resistance of an inverting amplifier are 3 and 12 kΩ respectively. If a voltage of 500 mV is applied to it, the output voltage and input voltage will be:

7 (A) Explain the working of a Cole strip oscillator with the help of a suitable circuit. Recall the input frequency and the necessary conditions for self-excited and self-sustained oscillations.

7 (B) Prove that for fed oscillations in an RC phase-shifted oscillator, $h_{fe} \ge 56$, where the symbols have their usual meaning.

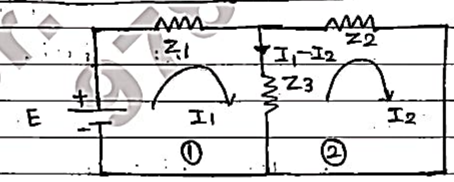
8 (A) 1 8 (B) Write circuit symbols and verification tables for NAND and XOR gates.

1. Reciprocity Theorem:-

⇒ Circuit which are designed from Biletral impidence there reciprocity theorm is valid.

"If Electric source is connect in first loop of network and due to which flow of electric current in loop II is I. Now If Electric source is connect in second loop then flow of electric current in Ist loop will be I."

Mathematical Verification:-



To do the mathematical Verification of Reciprocity theorm. A circuit designed by Biletral impidence network is used. let this Network is defined by Z_1, Z_2, Z_3. in this network a Voltage E is present. Due to this voltage flow of current in loop 1 is I_1 and flow of electric current in

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second loop is I_2.

From loop Analysis theorm.

$$\begin{bmatrix} Z_1+Z_3 & -Z_3 \\ -Z_3 & Z_2+Z_3 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} E \\ 0 \end{bmatrix}$$

$$[Z][I] = [E]$$

$$\Delta_Z = \begin{vmatrix} Z_1+Z_3 & -Z_3 \\ -Z_3 & Z_2+Z_3 \end{vmatrix}$$

$$\Delta_Z = (Z_1+Z_3)(Z_2+Z_3) - Z_3^2$$

$$\Delta_Z = Z_1Z_2 + Z_1Z_3 + Z_2Z_3 + Z_3^2 - Z_3^2$$

$$\boxed{\Delta_Z = Z_1Z_2 + Z_1Z_3 + Z_2Z_3}$$

Now

$$\Delta_1 = \begin{vmatrix} E & -Z_3 \\ 0 & Z_2+Z_3 \end{vmatrix}$$

$$\Delta_1 = (Z_2+Z_3)E$$

$$I_1 = \frac{\Delta_1}{\Delta_Z}$$

$$\boxed{I_1 = \frac{(Z_2+Z_3)E}{\Delta_Z}} \quad \text{--- ①}$$

Now

$$\Delta_2 = \begin{vmatrix} Z_1+Z_3 & E \\ -Z_3 & 0 \end{vmatrix}$$

$$\Delta_2 = +Z_3E$$

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$$I_2 = \frac{\Delta_2}{\Delta z}$$

$$\boxed{I_2 = \frac{+Z_3E}{\Delta z}} \quad \text{--- (2)}$$

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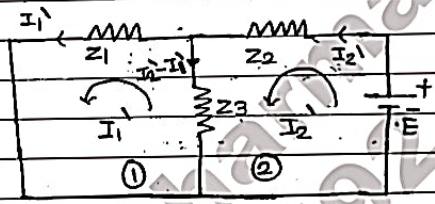
Step – II



Now we connect the electric source in 2nd loop due to which flow of electric current in 1st loop is I_1' and in second loop flow of electric current is I_2'.

From loop Analysis Theorem

$$\begin{bmatrix} Z_1+Z_3 & -Z_3 \\ -Z_3 & Z_2+Z_3 \end{bmatrix} \begin{bmatrix} I_1' \\ I_2' \end{bmatrix} = \begin{bmatrix} 0 \\ E \end{bmatrix}$$

$$[Z][I] = [E]$$

$$\Delta z = \begin{vmatrix} Z_1+Z_3 & -Z_3 \\ -Z_3 & Z_2+Z_3 \end{vmatrix}$$

$$\Delta z = (Z_1+Z_3)(Z_2+Z_3) - Z_3^2$$

$$\Delta z = Z_1Z_2 + Z_1Z_3 + Z_2Z_3 + Z_3^2 - Z_3^2$$

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$$\boxed{\Delta z = Z_1Z_2 + Z_1Z_3 + Z_2Z_3}$$

Now

$$\Delta_1 = \begin{vmatrix} 0 & -Z_3 \\ E & Z_2+Z_3 \end{vmatrix}$$

$$\boxed{\Delta_1 = EZ_3}$$

$$I_1' = \frac{\Delta_1}{\Delta z}$$

$$\boxed{I_1' = \frac{EZ_3}{\Delta z}} \quad \text{--- (3)}$$

From eqn (2) and (3)

$$\boxed{I_2 = I_1'}$$

Therefore, This is the Reciprocity Theorem.

V) ...

For a P-N junction determine the applied forward voltage when when $J_s = 30\ \mu A/cm^2$ and $J = 2 A/cm^2$ $(e/kT = 40/V)$. The notations have their usual meaning. **[R.U. 2006, 2010]**

हल–P–N डायोड में प्रवाहित धारा घनत्व

$$J = J_s\left[\exp\left(\frac{eV}{kT}\right) - 1\right]$$

प्रश्नानुसार, $J = 2\ A/cm^2$

$$J_s = 30\ \mu A/cm^2$$

$$\frac{eV}{kT} = 40\ /\ V$$

$$\therefore \quad \exp\left(\frac{eV}{kT}\right) - 1$$

$$= \frac{J}{J_s} = \frac{2}{30 \times 10^{-6}} = \frac{2}{3} \times 10^5$$

$$\therefore \quad \exp\left(\frac{eV}{kT}\right) \approx \frac{2}{3} \times 10^5$$

$$\frac{eV}{kT} = \log_e \frac{2}{3} \times 10^5$$

$$\therefore \quad V = \frac{kT}{e} \log_e \frac{2}{3} \times 10^5$$

$$V = \frac{2.3026 \times 4.8240}{40}$$

या $V = 0.28\ V$

5474

BIAS STABILITY :

Bias stabilization: While designing the biasing circuit, care should be taken so that the operating point will not shift into an undesirable region (i.e into cut-off or saturation region)

Factors to be considered while designing the basing circuit:

- Ico
- V_{BE}
- Beta

Factors to be considered while designing the basing circuit:

→ Temperature dependent factors (I_{CO}, V_{BE})
→ $\beta | hfe$ – Transistor current gain

I_{CO}:

The flow of current in the circuit produces heat at the junctions. This heat increases the temperature at the junctions.

Since the minority carriers are temperature dependent (I_{CO} gets doubled for energy 10°C raise in temperature), they increase with the temperature.
This in turn increase the I_C and hence Q – point gets shifted

V_{BE}:

→ V_{BE} changes with temperature at the rate of 2.5mv°/c
→ I_B depends on V_{BE}

Since $\frac{I_C}{I_B} = \beta$

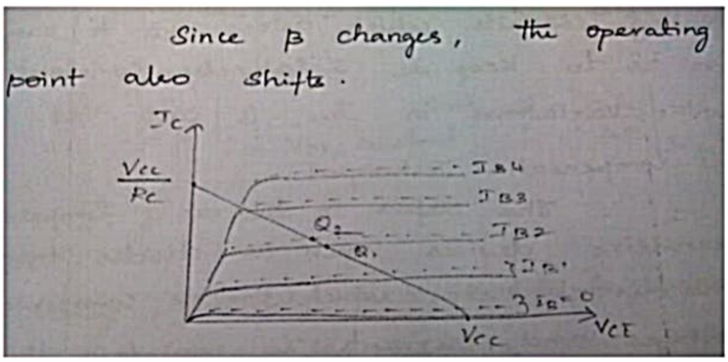
$I_C = \beta I_B$, increase in I_B

Increase I_C This in turn changes the operation point.

Transistor current gain β:

The transistor parameters among different units of same type, same number changes. Ie. If we take two transistor units of same type (ie. Same number, construction, parameter specified etc.) and we them in the circuit, there is change in the β value in actual practice.

The biasing circuit is designed according to the required β value.
Since β changes, the operating point also shifts.



Requirements of a biasing network:

- The emitter-base junction must be forward biased and collector-base junction must be reversed biased. i.e. The transistors should be operated in the active region.
- The circuit design should provide a degree of temperature stability.
- The operating point should be made independent of transistor parameters (like transistor current gain)

Techniques used to keep Q point stable:

STABILIZATION TECHNIQUE:

This refers to the use of resistive biasing circuits which allow I_B to vary so as to keep I_C Relatively constant with variations in I_{CO} and V_{BE} current gain(beta)

COMPENSATION TECHNIQUE:

This refers to the use of temperature sensitive devices such as diodes, transistors, thermistors, etc, which provide compensating voltages and current to maintain the operating point stable.

Stability Factors :

STABILITY FACTORS:

- The stability factor is a measure of stability provided by the biasing circuit.
- Stability factor indicates the degree of change in operating point due to variation in temperature.
- Since there are 3 temperature dependent variables, there are 3 stability factors.

$S = \frac{\partial I_C}{\partial I_{CO}} |V_{BE.\beta\ constant}$ (or) $S = \frac{\Delta I_C}{\Delta I_{CO}} |V_{BE.\beta\ constant}$

$S' = \frac{\partial I_C}{\partial V_{BE}} |I_{CO.\beta\ constant}$ (or) $S' = \frac{\Delta I_C}{\Delta V_{BE}} |I_{CO.\beta\ constant}$

$S'' = \frac{\partial I_C}{\partial \beta} |V_{BE.I_{CO}\ constant}$ (or) $S'' = \frac{\Delta I_C}{\Delta \beta} |V_{BE.I_{CO}\ constant}$

Note:

- Ideally, stability factor should be perfectly zero to keep the operating point stable.
- Practically stability factor should have the value as minimum as possible.

EXPRESSION FOR STABILITY FACTOR S:

For a common emitter configuration collector current is given by

$I_C = I_{C(majority)} + I_{CEO\,(majority)}$

WKT

$I_{CEO} = \frac{I_{CBO}}{1 - \alpha}$

$I_{CEO} = (1 + \beta)\, I_{CBO}$

$I_C = \beta I_B + (1 + \beta)\, I_{CBO}$

When
I_{CBO} changes by ΔI_{CBO}
I_B changes by ΔI_B
I_C changes by ΔI_C

$\partial I_C = \beta \partial I_B + (1 + \beta) \partial I_{CBO}$

÷ by ∂I_C

$1 = \beta \frac{\partial I_B}{\partial I_C} + (1 + \beta) \frac{\partial I_{CBO}}{\partial I_C}$

$1 - \beta \frac{\partial I_B}{\partial I_C} = (1 + \beta) \frac{\partial I_{CBO}}{\partial I_C}$

$\frac{\partial I_{CBO}}{\partial I_C} = \frac{(1 - \beta)\frac{\partial I_B}{\partial I_C}}{(1 + \beta)}$

If $S = \frac{\partial I_C}{\partial I_{CBO}}$

$\frac{1}{S} = \frac{(1 - \beta)\frac{\partial I_B}{\partial I_C}}{(1 + \beta)}$

$$\boxed{S = \frac{(1 + \beta)}{(1 - \beta)\frac{\partial I_B}{\partial I_C}}}$$

If current gain in CB mode of a transistor is 0.98 then find current gain in CE mdoe and CC mode. [Ajmer 2016]

हल: दिया हुआ है $\alpha = 0.98$

हम जानते हैं $\beta = \dfrac{0.98}{1-0.98} = \dfrac{0.98}{0.02} = 49$

CC विन्यास में धारा लाभ

$$\gamma = 1+\beta = 1+49 = 50$$

4 NAND-logic Gate :-

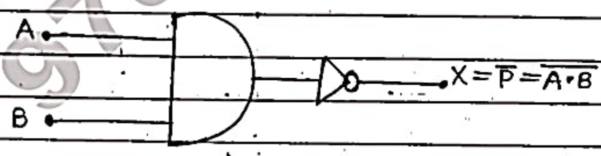
This is a combinational logic gate. This logic gate is combined form of NOT + AND = NAND so,

NOT + AND = NAND

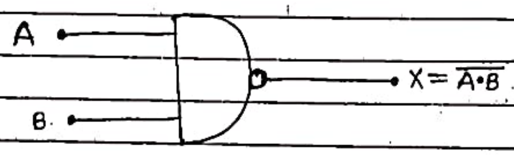
ⓐ Boolean function :-

$X = \overline{A \cdot B}$

ⓑ Symbol :-



OR



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ⓒ Truth Table :-

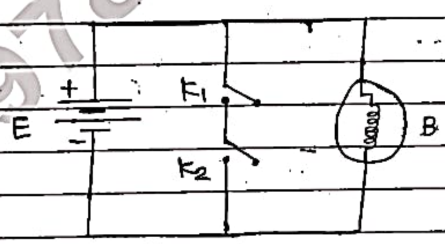
A	B	A·B	$X = \overline{A \cdot B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

ⓓ Definition :-

That logic gate in which at every point of input terminal ON state is their then OFF state is find on output terminal. Then it is called NAND logic gate.

That logic gate in which at any point of input terminal OFF state is their then ON state is find on output terminal is called NAND logic gate.

ⓔ Switch circuit :-



XOR-Logic Gate :-

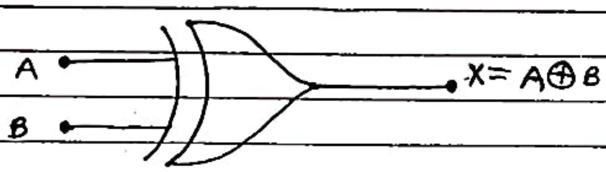
This logic gate is said to be exclusive logic gate.

ⓐ Boolean function :-

$$X = A \oplus B$$

$$X = (A+B) \cdot (\overline{A \cdot B})$$

ⓑ Symbol



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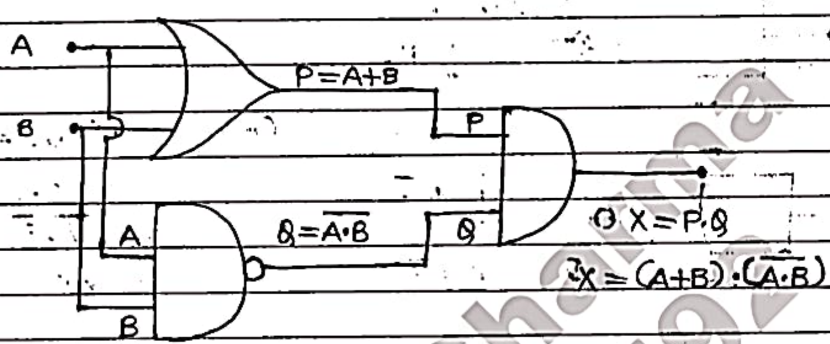
ⓒ Switch circuit :-

$$X = (A+B) \cdot (\overline{A \cdot B}) \quad \text{—— ①}$$



ⓓ Truth Table

A	B	A+B	A·B	$\overline{A \cdot B}$	$X = (A+B) \cdot (\overline{A \cdot B})$
0	0	0	0	1	0
0	1	1	0	1	1
1	0	1	0	1	1
1	1	1	1	0	0

ⓔ Defination :-

This is a special type of OR gate in which two input terminal (2) and single (1) output terminal exists is called XOR-logic gate.

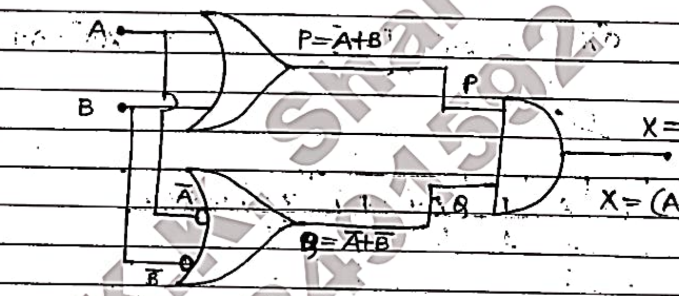
"That logic gate in which OFF state means zero find on giving same input signal and ON state finds when different input signal is given."

© circuit (2) :- From eqⁿ(1)

$$X = (A+B)\cdot(\overline{A\cdot B})$$

From Demorgan's theorem

$$\boxed{X = (A+B)\cdot(\bar{A}+\bar{B})} \quad —— (2)$$



A	B	$\bar{A}$	$\bar{B}$	A+B	$\bar{A}+\bar{B}$	$X=(A+B)\cdot(\bar{A}+\bar{B})$
0	0	1	1	0	1	0
0	1	1	0	1	1	1
1	0	0	1	1	1	1
1	1	0	0	1	0	0

© Circuit-3

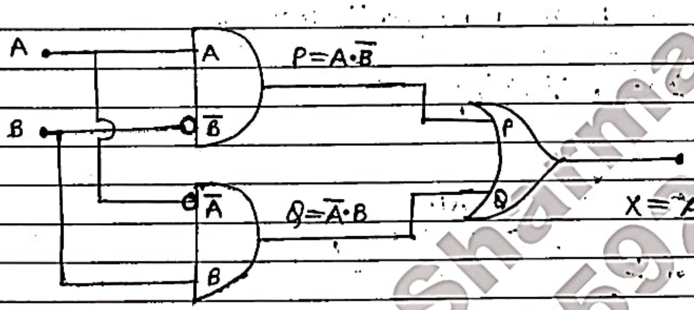
From eqⁿ(2)

$$X = (A+B)\cdot(\bar{A}+\bar{B})$$

$$X = A\cdot\bar{A} + A\cdot\bar{B} + B\cdot\bar{A} + B\cdot\bar{B}$$

$$\because \quad A\cdot\bar{A} = B\cdot\bar{B} = 0$$

$$\boxed{X = A\cdot\bar{B} + B\cdot\bar{A}} \quad —— (3)$$



A	B	$\bar{A}$	$\bar{B}$	$A\cdot\bar{B}$	$B\cdot\bar{A}$	$X=A\cdot\bar{B}+B\cdot\bar{A}$
0	0	1	1	0	0	0
0	1	1	0	0	1	1
1	0	0	1	1	0	1
1	1	0	0	0	0	0

Solution

$$\left[A\bar{B}(C+BD)+\overline{AB}\right]C$$

$$\left[A\bar{B}C+A\bar{B}BD+\overline{AB}\right]C$$

$$\left[A\bar{B}C+\bar{A}+\bar{B}\right]C \quad \because B\bar{B}=0$$

$$\left[\bar{A}+\bar{B}(1+\bar{A}C\right]C$$

$$\left[\bar{A}+\bar{B}\right]C$$

$$\bar{A}C+\bar{B}C$$

Adder:

Op-amp may be used to design a circuit whose output is the sum of several input signals.Such a circuit is called a summing amplifier or a summer or adder.An inverting summer or a non-inverting summer may be discussed now.

Inverting Summing Amplifier:

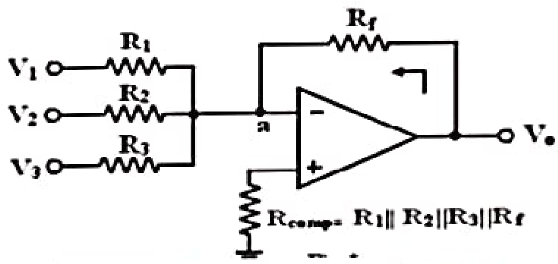


Fig 1.Inverting summer(source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/)

A typical summing amplifier with three input voltages V_1, V_2 and V_3 three input resistors R_1, R_2, R_3 and a feedback resistor R_f is shown in fig1.The following analysis is carried out assuming that the op-amp is an ideal one, AOL= ∞.Since the input bias current is assumed to be zero, there is no voltage drop across the resistor R_{comp} and hence the non-inverting input terminal is at ground potential.

$$I= V_1/R1+V_2/R2.....+Vn/Rn;$$

$$Vo= - R_f$$

$$I=Rf/R(V_1+V_2+....V_n).$$

To find R_{comp}, make all inputs $V_1 = V_2 = V_3 = 0$.

So the effective input resistance $R_i = R_1 \| R_2 \| R_3$.

Therefore, $Rcomp = R_i \| R_f = R_1 \| R_2 \| R_3 \| R,f$.

Non-Inverting Summing Amplifier:

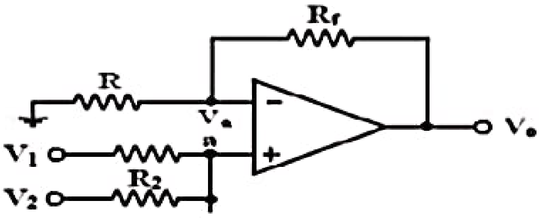


Fig 2.non-inverting summer (source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/)

A summer that gives a non-inverted sum is the non-inverting summing amplifier of fig 2. Let the voltage at the (-) input terminal be Va. which is a non-inverting weighted sum of inputs.

Let $R_1 = R_2 = R_3 = R = R_f/2$, then $V_o = V_1+V_2+V_3$

Subtractor using Operational Amplifier

If all resistors are equal in value, then the output voltage can be derived by using superposition principle.

Subtractor:

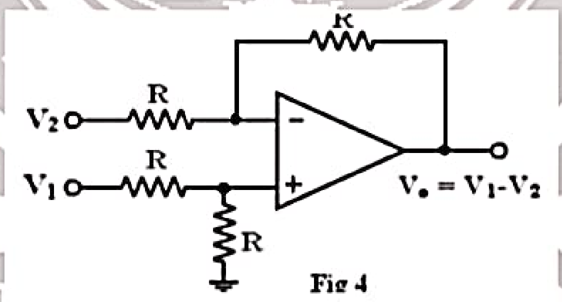


Fig 3.Subtractor (source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/)

A basic differential amplifier can be used as a subtractor as shown in the above fig 3. If all resistors are equal in value, then the output voltage can be derived by using superposition principle.

To find the output V_{01} due to V_1 alone, make $V_2 = 0$.

Then the circuit of figure as shown in the above becomes a non-inverting amplifier having input voltage $V_1/2$ at the non-inverting input terminal and the output becomes

$V_{01} = V_1/2(1+R/R) = V_1$ when all resistances are R in the circuit.

Similarly the output V_{02} due to V_2 alone (with V_1 grounded) can be written simply for an inverting amplifier as

$V_{02} = -V_2$

Thus the output voltage Vo due to both the inputs can be written as

$V_0 = V_{01} - V_{02} = V_1 - V_2$

Adder/Subtractor:

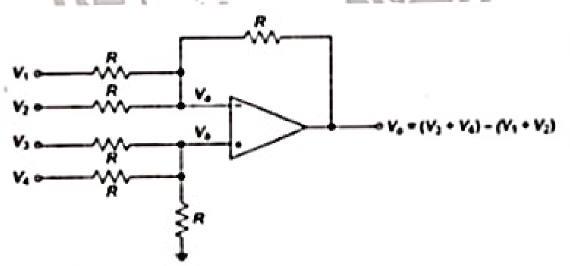


Fig 4 a) Adder-Subtractor(source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/)

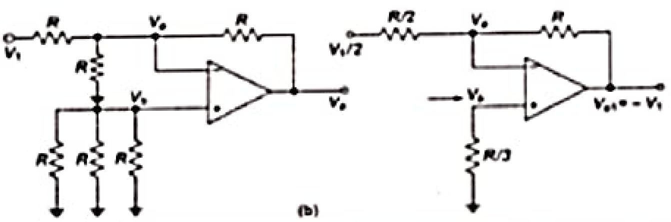


Fig4 b)Equivalent circuit for V2=V3=V4=0(source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/)

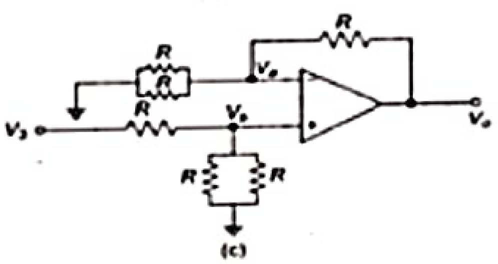


Fig 4 c) Equivalent circuit for V1=V2=V4=0(source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/)

It is possible to perform addition and subtraction simultaneously with a single op-amp using the circuit shown in fig 4 a) The output voltage Vo can be obtained by using superposition theorem. To find output voltage V_{01} due to V_1 alone, make all other input voltages V_2, V_3 and V_4 equal to zero. The simplified circuit is shown in fig 4 b). This is the circuit of an inverting amplifier and its output voltage is, $V_{01}= -R/(R/2) * V_1/2= - V_1$ by Thevenin's equivalent circuit at inverting input terminal).Similarly, the output voltage V_{02} due to V_2 alone is,

$$V_{02}= - V_2$$

Now, the output voltage V_{03} due to the input voltage signal V_3 alone applied at the (+) input terminal can be found by setting V_1, V_2 and V_4 equal to zero.

$$V_{03}=V_3$$

The circuit now becomes a non-inverting amplifier as shown in fig.4(c).
So, the output voltage V_{03} due to V_3 alone is

$$V_{03} = V_3$$

Similarly, it can be shown that the output voltage V_{04} due to V_4 alone is

$$V_{04} = V_4$$

Thus, the output voltage Vo due to all four input voltages is given by

$$V_o = V_{01} = V_{02} = V_{03} = V_{04}$$

$$Vo = - V_1 -V_2 +V_3+ V_4$$

$$V_o = (V_3 +V_4) - (V_1 +V_2)$$

So, the circuit is an adder-subtractor.

The CMRR of a differential amplifier is 55 dB. If its differential mode gain is 1200, determine the common-mode gain.

5 (B)

हल–प्रश्नानुसार

$$A_d = 1200$$

डेसिबेल में

$$CMRR = 20\log_{10}\frac{A_d}{A_c} = 55$$

$$\therefore \quad \frac{A_d}{A_c} = \text{Anti}\log_{10}\frac{55}{20} = 562.3$$

$$A_c = \frac{A_d}{562.3} = \frac{1200}{562.3} = 2.13$$